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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/681,675	10/06/2003	Hugo Cheung	38880.7100	7689

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EXAMINER

BUTLER, DENNIS

ART UNIT	PAPER NUMBER
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2115

DATE MAILED: 04/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/681,675

Applicant(s)

CHEUNG ET AL.

Examiner

Dennis M. Butler

Art Unit

2115

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 October 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 5, 6 and 8 is/are allowed.
- 6) ☒ Claim(s) 1-4, 7, 9 and 10 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 06 October 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

1. This action is in response to the application filed on October 6, 2003. Claims 1-10 are pending.

2. The drawings are objected to because they are informal. See attached form PTO-948. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 3, 7 and 9 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 3 and 7, the phrase "which equal are of" is unclear as to its meaning and its relationship to the divisor values.

Regarding claim 9, the claim is unclear as to the relationship of the medium mode and the divider because no relationship is recited.

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 1 and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Dallas Semiconductor DS1075 EconOscillator/Divider.

Per claim 1:

A) Dallas Semiconductor teaches the following claimed items:

1. a divider register storing a mode indicator (DIV1) and a divisor indicator (N) with EEPROM of figure 1 on page 2, with MUX WORD of figure 2 on page 4, with DIV WORD of figure 3 on page 5 and with the USER –PROGRAMMABLE REGISTERS section on pages 3-5;
2. a divider accepting a first clock having a first frequency (Internal Oscillator) and producing a second clock having a second frequency (IN/OUT clock output), the divider having a normal mode and a divide mode selectable via a mode indicator with PROGRAMMABLE DIVIDER of figure 1 on page 2 and with the DESCRIPTION section on page 1;
3. a normal mode where the second frequency is substantially the same as the first frequency with the DIV1=1 programmable divider bypass mode and the DIV1 section on page 4;
4. a divide mode where the second frequency is less than the first frequency by a divisor value corresponding to the divisor indicator with the DIV1=0 programmable divider mode and the N section on page 5.

Per claim 10:

A) Dallas Semiconductor teaches the following claimed items:

1. a register configured to store a divisor indicator with EEPROM of figure 1 on page 2, with MUX WORD of figure 2 on page 4, with DIV WORD of figure 3 on page 5 and with the USER –PROGRAMMABLE REGISTERS section on pages 3-5;
 2. a divider accepting a first clock having a first frequency (Internal Oscillator) and producing a second clock having a second frequency (IN/OUT clock output) with PROGRAMMABLE DIVIDER of figure 1 on page 2 and with the DESCRIPTION section on page 1;
 3. a normal mode where the second frequency is substantially the same as the first frequency with the DIV1=1 programmable divider bypass mode and the DIV1 section on page 4;
 4. a divide mode where the second frequency is less than the first frequency by a divisor value corresponding to the divisor indicator with the DIV1=0 programmable divider mode and the N section on page 5.
9. Claims 2-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dallas Semiconductor DS1075 EconOscillator/Divider.

Per claims 2-4:

Dallas Semiconductor teaches the elements of claim 1 as described above. The claims differ from Dallas Semiconductor in that Dallas Semiconductor fails to explicitly teach providing the divisor values as recited in claims 2-4. Dallas Semiconductor discloses linking desired divisor values to binary numbers with table 3 and with the N section on page 5. The divisor values that are linked to the

binary numbers are a design choice that is based on the desired operating characteristics of the system. It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide multiple divisors that are multiples of two in order to provide a wide range of clock signals for operating over a wide range of system operating characteristics including power saving characteristics and performance tuning characteristics.

10. Claims 1-4 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over White, U. S. Patent 3,867,614.

Per claim 1:

A) White teaches the following claimed items:

1. a divider accepting a first clock having a first frequency (the clock output on line 22) and producing a second clock having a second frequency (the clock output on line 40), the divider having a normal mode and a divide mode selectable via a mode indicator with divider 30 of figure 1 and at column 3, line 38 – column 4, line 28;
2. a normal mode where the second frequency is substantially the same as the first frequency with the bypass mode (M1 and M2 both equal 1) at column 4, lines 4-11;
3. a divide mode where the second frequency is less than the first frequency by a divisor value corresponding to the divisor indicator with the mode corresponding to the first three conditions in truth table 39 of figure 1 and at column 3, line 54 – column 4, line 3.

B) The claims differ from White in that White fails to explicitly teach a divider register storing a mode indicator and a divisor indicator as claimed.

C) However, White describes a memory configured to store a mode indicator ($M1=1$ and $M2=1$) a divisor indicator ($M1$ and $M2$ not both equal to 1) with terminals $M1$ and $M2$ of figure 1 and at column 3, lines 38-42. Therefore, White discloses the claimed invention except for explicitly reciting that memory locations $M1$ and $M2$ are in a register. However, registers are a well known type of memory in the data processing art and it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify White's programmable counter by replacing memory locations $M1$ and $M2$ with corresponding register memory locations $M1$ and $M2$ in order to reduce the switching circuitry (switch 36 and switch 38) and size of the circuit while maintaining programmable divider operation as shown in truth table 39 of figure 1.

Per claims 2-4:

White discloses linking desired divisor values to binary numbers with truth table 39 of figure 1 and at column 3, lines 53-56. The divisor values that are linked to the binary numbers are a design choice that is based on the desired operating characteristics of the system. It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide multiple divisors that are multiples of two in order to provide a wide range of clock signals for operating

over a wide range of system operating characteristics including power saving characteristics and performance tuning characteristics.

Per claim 10:

A) White teaches the following claimed items:

1. a divider accepting a first clock having a first frequency (the clock output on line 22) and producing a second clock having a second frequency (the clock output on line 40) with divider 30 of figure 1 and at column 3, line 38 – column 4, line 28;
2. a normal mode where the second frequency is substantially the same as the first frequency with the bypass mode (M1 and M2 both equal 1) at column 4, lines 4-11;
3. a divide mode where the second frequency is less than the first frequency by a divisor value corresponding to the divisor indicator with the mode corresponding to the first three conditions in truth table 39 of figure 1 and at column 3, line 54 – column 4, line 3.

B) The claims seem to differ from White in that White fails to explicitly teach a register configured to store a divisor indicator as claimed.

C) However, White describes a memory configured to store a divisor indicator with terminals M1 and M2 of figure 1 and at column 3, lines 38-42. Therefore, White discloses the claimed invention except for explicitly reciting that memory locations M1 and M2 are in a register. However, registers are a well known type of memory in the data processing art and it would have been obvious to one

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having ordinary skill in the art at the time the invention was made to modify White's programmable counter by replacing memory locations M1 and M2 with corresponding register memory locations M1 and M2 in order to reduce the switching circuitry (switch 36 and switch 38) and size of the circuit while maintaining programmable divider operation as shown in truth table 39 of figure 1.

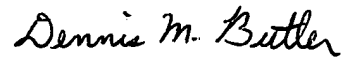
11. Claims 5, 6 and 8 are allowable over the art of record because the art of record does not teach or suggest a system clock divider including a divider having a normal mode and first and second divide modes wherein the normal mode produces the second frequency substantially the same as the first, the first divide mode produces the second frequency that is less than the first frequency by a divisor value corresponding to the divisor indicator and the second divide mode produces the second frequency that is less than the first frequency by a divisor value corresponding to the divisor indicator and the second divide mode is entered and/or exited through the use of a user countable millisecond interrupt signal as recited in independent claim 5.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dennis M. Butler whose telephone number is 571-272-3663. The fax number for this unit is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

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For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Dennis M. Butler
Primary Examiner
Art Unit 2115